Fast Calculation of System-Level ESD Noise Coupling to a Microstrip Line Using PEEC Method

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Abstract—The system-level ESD coupling on a microstrip line is calculated using the partial element equivalent circuit (PEEC) method both in frequency and time domains. A simplified MNA matrix for the victim trace is proposed to quickly calculate the charge and current induced due to the ESD event. The calculated coupling transfer impedance and the ESD waveforms coupled on the traces are validated by comparison with measurements both in frequency and time domains.

Keywords—Electrostatic discharge (ESD); partial element equivalent circuit (PEEC); microstrip line; modified nodal analysis (MNA)

I. INTRODUCTION

Electrostatic discharge (ESD) is one of the most critical noisy events on integrated circuits (ICs) in an electronic system, as depicted in Fig. 1. Since the ESD events create a high current peak with fast rise time, it can cause unexpected large noise coupled on signal traces and result in malfunctions of ICs, although ICs are basically designed to be immune to external noises. It is difficult to expect the amount and coupling path of the ESD noise and how it causes functional failures in ICs. For system-level ESD simulations, several electromagnetic (EM) numerical methods, such as the finite-difference time-domain (FDTD) and finite integration technique (FIT), have been utilized to calculate the noise coupling due to ESD events [1]-[2].

Recently, the partial element equivalent circuit (PEEC) method has also been applied to efficiently calculate ESD noise coupling to simple victim structures, such as a conductor loop and floating two metal pieces [3], [4]. There are several advantages of PEEC method for ESD simulation. First, the ESD generator R-C circuit model can be easily incorporated into the PEEC method. Second, the ESD source can be realized by the ESD initial voltage condition using PEEC method, while it is modeled as the voltage step function with a short rise time using commercial full-wave solvers. Due to the limited rise time of the voltage step function, the ESD simulation results using the FDTD method is very sensitive to the mesh size. Another advantage is that small victim structures can be separately handled from the large ESD grounds using the PEEC method. However, in the previous works [3] and [4], just one coupling source of current or charge was used to calculate the ESD noise on each inductive or capacitive victim structure, which is not realistic geometry in a practical electronic system.

Assuming that the reverse effect from the small victim to the large aggressor geometry such as ground planes is negligible, the modified nodal analysis (MNA) matrix for only victim structure can be simply obtained. Using the MNA matrix for a microstrip line, the coupled voltage across the 50Ω terminations at the ends of microstrip line is calculated and validated with measurements both in frequency and time domain.

II. GEOMETRIES FOR MEASUREMENTS OF ESD NOISE COUPLING

For the measurements of the ESD noise coupling, a test PCB with single microstrip line was designed and fabricated. As shown in Fig. 2(a), the both ends of the microstrip line with 20 mm-length are connected to the SMA connector for measurements. The trace width is 1 mm and the FR-4 material with 3.2 mm height fills between the trace and the PCB ground plane. Four victim positions shown in Fig. 2(b)-(e) are chosen to investigate the effect of the trace positions. Each termination voltages of the trace are named as V1 and V2. The voltage of V1 is calculated and measured.
Fig. 2. Test PCB geometry with four victim positions (a) side view (b) position a (c) position b (d) position c (e) position d.

Two ESD test setups are designed as shown in Fig. 3. The ESD event is excited at a PCB ground plane in both cases. In the ‘case A’ of Fig. 3 (a), one end of the gun strap is connected to the PCB ground plane, and the other is connected to the return path of the ESD current source. In the ‘case B’ of Fig. 3 (b), one end of gun strap is connected to the additional large ESD test ground plane located below the test PCB, and the other is also connected to the return path of the ESD current source. The PCB is isolated from the large ground plane by a thin insulating material. The case B would be a more realistic condition for the system-level ESD immunity test.

Fig. 3. Two ESD test setups (a) case A : the gun strap is connected to PCB ground plane (b) case B : the gun strap is connected to a larger plane under the PCB.

III. PEEC MNA MATRIX FOR NOISE COUPLING TRANSFER IMPEDANCE CALCULATION IN FREQUENCY DOMAIN

The key point of noise calculation using PEEC method is that the victim geometry is separately handled from the total structure. A new MNA matrix for only the victim geometry is built to consider all of the inductive, capacitive, and conductive couplings on the microstrip line. The subscript notations $a$ and $v$ are used herein to represent the aggressor and the victim structures, respectively. For example, $P_{av}$ means the potential coefficient matrix including retardation effect from the aggressor to the victim. The potential coefficients and partial inductances are referred to in [5]-[9].

Fig. 4. Model of the victim and a part of aggressor structures

The victim and a part of aggressor structures are illustrated in Fig. 4. The $V_L$ and $V_R$ represent the voltages at the termination points on the aggressor. The $I_L$ and $I_R$ represent the current flowing through the trace terminations. The $Q_{av}$, $I_{av}$, $Q_v$, and $I_v$ represents the charge and current vectors at the aggressor and the victim, respectively. The KCL and KVL at the internal nodes and branches in the victim are then written as, respectively,

$$s \bar{E} Q_v + I_{av} T_v = 0$$  
$$V_v = s L_{av} I_v + s I_{av} T_a = 0$$  
$$aavvvvv QPsQPsV = 0$$

Also, the KCL and KVL at the termination nodes and branches of the victim are given as,

$$s \bar{E} Q_v + I_{av} T_v + N_L^T I_L + N_R^T I_R = 0$$

Assuming that the reverse coupling effects from the victim to the aggressor is negligible, the charge and current of the aggressor, $Q_a$ and $I_a$, can be solved in advance using the MNA matrix with only the aggressor structure [3], [4]. After solving the aggressor structure at first, the MNA matrix for the $Q_v$ and $I_v$ of the victim geometry is constructed as (7), where the $Q_a$ and $I_a$ behave as sources in the right side of victim MNA matrix. The assumption, however, could degrade the calculation accuracy considerably in this case, since the transmission characteristics of the microstrip line basically involves the interaction between the trace and the reference ground plane.

For the validation of the coupling model in frequency domain, the transfer impedance between the aggressor excitation current and the victim termination voltage $V_1$ is calculated using (7) and measured using the vector network analyzer (VNA). The SMA port connection for the
measurements is shown in Fig. 5. The both ends of the microstrip line are terminated to the PCB ground through 51Ω chip resistors on the back side of the PCB. In both cases, the calculated transfer impedances at all four victim positions are compared with measurements.

Fig. 5. SMA port connections in the VNA measurements

Fig. 6 shows the transfer impedance from PEEC calculation and measurement. Fig. 6(a) represents the PEEC calculation and measurement for case A, respectively. Fig. 6(b) represents the PEEC calculation and measurement for case B. In the case A which has inductive return path, the coupling transfer impedance has the inductive curve at low frequency region. On the other hand, in the case B which has capacitive return path, the coupling transfer impedance has a flat curve at low frequency. The trends and relative levels agree between PEEC and measurements except at impedance peaks and low frequency region in the case B. The low frequency error in the case B is attributed to the neglect of the reverse coupling effects from the victim to the aggressor. The transfer impedance in each victim cases can be calculated very fast using the proposed calculation method. To calculate the aggressor structure in case B at 801 frequency points from 3 kHz to 1 GHz, it takes 2 hr 32 min 20 sec. The calculation for one victim position in case B, however, takes just 12.3 sec using the aggressor results. In all computation, a desktop PC with 12GBytes memory and 3.3 GHz CPU was used.

IV. CALCULATION OF TRANSIENT ESD COUPLED WAVEFORM IN TIME DOMAIN

The contact-mode ESD calculation involves predominantly only linear models, and the solution in frequency domain can be converted to time domain by the inverse Fourier transform, which can provide more stable solution than direct time-domain PEEC calculation [10]. To obtain the ESD coupling results in time domain, the current and charge distribution on the aggressor are calculated with the ESD initial voltage condition in frequency domain [3], [4]. According to the international standard of the contact discharging model ESD [11], the ESD generator is modeled as R-C circuits of 330Ω and 150 pF, and inserted at the ESD injection point. The ESD gun capacitance is initially charged to an ESD initial voltage, such as 2kV, and discharged through the total aggressor structure. The charges and currents in the aggressor structure are calculated at first, and used to find the voltage and currents at the victims by (7). Finally, the calculated voltage spectrum is converted to the time domain.

The time-domain measurement setup is shown in Fig. 7. The both ends of microstrip line are terminated to 50Ω. One end is connected to the 50Ω termination in the oscilloscope and the other end is terminated to a SMA 50Ω terminator.
Fig. 7. ESD measurement setup. (a) total configuration (b) the conditions of 50Ω termination for ESD test.

Fig. 8 shows the calculated and measured voltage waveforms at the victim V1 termination induced by the 2kV ESD event. As examples, the waveforms at the victim position b are shown for both case A and B. The ESD transient results are also quite similar between the PEEC calculation and the measurements. The transfer impedances at low frequency in the case B is higher than those in the case A. However, since the dominant component of ESD coupled noise is at high frequencies, the transient coupling noise peak in the case A is higher than that in the case B. Also, compared to the victim structure of a conductor loop in [4], the ESD coupling noise is lower in the microstrip victim used herein. For example, for the position b in the case A, the peak noise voltage is 1.441V in the microstrip line victim while it is 1.877V in the conductor loop victim.

Fig. 8. ESD coupling waveforms at the V1 termination; (a) position b in case A (b) position b in case B

V. CONCLUSION

The system-level ESD couplings on a microstrip line were calculated and measured. The simplified MNA matrix for the microstrip line was proposed to calculate the charge and current induced due to the ESD event. The coupling transfer impedance at the trace terminations were calculated in frequency domain and validated by the VNA measurements. Also, the transient voltage waveforms at the trace induced by 2kV ESD events were calculated in time domain and validated with ESD measurements. The ESD coupling voltages at various trace positions can be calculated very fast using the proposed calculation, however, there is a limitation in accuracy, since the reverse coupling effects from the victim to the aggressor was ignored.

REFERENCES