LTCC Package for High-bandwidth Logic to Memory Interconnection

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Abstract—Advancements in packaging technologies are required to meet the future bandwidth, and space- and energy-efficient demands of ICT systems. One of the key technologies is 2.5D packaging using a silicon interposer with through silicon vias (TSVs). However, forming the TSV and thinning the wafer makes the Si interposer’s cost high. Furthermore, using an organic substrate causes high electrical losses and warpage. We propose a low-temperature co-fired ceramics (LTCC) package with fine line layers to help alleviate these problems. The surface of the LTCC substrate is made very flat, so fine patterns with line/space that is 2/2μm can be formed. The LTCC package has been expected to decrease the necessary costs by simplifying the assembly process and introducing a panel-based process. Moreover, the LTCC substrate is more reliable than a Si interposer with an organic substrate and can transmit a high data rate signal at a lower loss. We demonstrated the possibility of high Bandwidth Memory (HBM) routing using the LTCC package.

Keywords—2.5D package; LTCC substrate; interposer; high-bandwidth memory;

I. INTRODUCTION

The era of big data now requires more powerful ICT systems. However, the performance gains when using semiconductors due to their traditional scaling is decreasing. Additionally, there are more complex circuit designs and the mask cost is increasing. So, advancements in the packaging technologies are required to meet the future bandwidth, and space- and energy-efficient demands of ICT systems.

One of the key technologies is 2.5D packaging, which uses a silicon interposer with through silicon vias (TSVs)[1]. Xilinx's FPGA achieves a high gate count and resource-rich FPGA when using a Si interposer [2], [3]. High Bandwidth Memory (HBM), which can achieve a high bandwidth/power efficient connection by using a fine Si interposer pattern set between the CPU or ASIC and stacked memories, has already been proposed and announced [4], [5].

The Si interposer is fabricated using the process discussed below. The TSVs are etched using the DRIE process to form a high aspect ratio via. Multi-layer wires are formed on the front side of the interposer using the standard Back-end-of-line (BEOL) process. After that, the backside of the wafer is thinned and C4 bumps are formed. Micro-bumps are formed at the top of the interposer and several chips are mounted on it. Finally, the interposer is assembled on a package substrate.

The Si interposer has a sub micron very fine patterning capability as a result of using the IC fabrication process. However, forming the TSVs and thinning the wafer makes the cost of making the Si interposer high. Furthermore, by using an organic substrate, it experiences high electrical losses in addition to the warpage caused by the coefficient of thermal expansion (CTE) mismatch between the interposer and the organic substrate.

We propose a low-temperature co-fired ceramics (LTCC) package with fine line layers to improve upon the current issues. The LTCC package with fine line layers is fabricated by forming thin film high density layers on an LTCC substrate. Its surface is made very flat, so it can be used to form fine patterns with line/space that is 2/2μm. The LTCC package can be used to simplify the assembly process. Moreover, the more packages can be produced at one time than from a circular wafer by introducing a panel-based process. Therefore, the LTCC package is expected to decrease costs.

Additionally, the LTCC substrate can provide a better electrical performance than organic materials, and its CTE (6 ppm) can strike a balance between the 1st and 2nd assembly.

II. STRUCTURE OF LTCC PACKAGE WITH FINE LINE LAYERS

Fig. 1 shows a cross section of the LTCC package with fine line layers.

![Fig. 1 Cross section of LTCC package with fine line layers](image)

The ceramics material used in the LTCC substrate has three key features. First, it is Pb free. Second is its transverse strength was improved up to 300 MPa by introducing a
controlled crystalline structure, which can reduce the decrease in density during sintering. A controlled crystalline structure also can decrease void and improve the surface flatness. Third, the use of zero shrink technology helped to decrease the amount of shrinkage in XY direction \cite{6}. These features help to form the fine line layer's patterns, which have a line/space of 2/2 μm and to form the fine line layer's vias which have a minimum pitch of 20 μm and a minimum diameter of 10 μm. Up to three fine line layers can be formed. The insulator is a polyimide and the conductor is Cu. The conductor of the LTCC substrate is Ag, the line/space is 30/30 μm, and the minimum diameter of a via is 60 μm. The LTCC layer can be comprised of up to 10 layers and still be coreless. Table 1 lists the design specifications of the fine line layer and LTCC layer.

<table>
<thead>
<tr>
<th></th>
<th>Unit</th>
<th>LTCC layer</th>
<th>Fine line layer</th>
</tr>
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<tbody>
<tr>
<td>Min. line &amp; space</td>
<td>μm</td>
<td>30/30</td>
<td>2/2</td>
</tr>
<tr>
<td>Min. via pitch</td>
<td>μm</td>
<td>120</td>
<td>20</td>
</tr>
<tr>
<td>Min. hole diameter</td>
<td>μm</td>
<td>60</td>
<td>10</td>
</tr>
<tr>
<td>Min. pad diameter</td>
<td>μm</td>
<td>70</td>
<td>12</td>
</tr>
</tbody>
</table>

Fig. 2 shows the process flow of the LTCC package with fine line layers.

The LTCC substrate is fabricated as follows. First, the ceramics sheet is molded. Then, the vias are formed using a laser and the electrode pattern is printed with the Ag. After that, the sheet is laminated and sintered. After that Polishing is used to flatten the surface of the LTCC substrate (Fig. 2(a)), and then, the resin is laminated (Fig. 2(b)), the vias are formed (Fig. 2(c)), the seed layer is sputtered (Fig. 2(d)), the pattern is transferred using photolithography (Fig. 2(e)), and a Cu electrode pattern is plated using an electrolytic (Fig. 2(f)). Steps (b) to (f) are repeated to form multi-layers.

### III. DESIGN STUDY OF HBM

HBM is composed of four stacked DRAMs and a base logic die. Each DRAM has two channels, where each channel provides 128 I/Os. Therefore HBM has 1024 I/Os. The JEDEC HBM standard specifies the HBM footprint, which contains 24 signal rows with a face-centered rectangular pattern. The specification of the pad pitch specify that the long-side direction pitch of a rectangle is 96 μm, and that the short-side and corner-center directions are 55 μm. Therefore, if eight row escape routing lines can be arranged between the pads with a 55 μm pitch, a fine line layer of up to three layers is sufficient in order to form the connection between the ASIC and HBM, as shown Fig. 3.

We fabricated a test vehicle to demonstrate the capabilities of HBM routing. A 25 × 25 mm, 8-layer LTCC substrate was used for the demonstration. Fig. 4 shows an over view image of the test vehicle.
IV. WARPAGE SIMULATION AND ANALYSIS

FEM-based simulations were used to analyze the warpage behavior of the LTCC package with fine line layers. Fig. 5(a) shows a top view of the model. The substrate is assumed to be \(50 \times 50\) mm, and a \(20 \times 20\) mm ASIC and four HBMs are mounted on it. The FEM models were created as half models. Fig. 5(b) shows a cross section of the model. We also created the Si interposer package model with the organic substrate for comparison. Fig. 5(c) shows a cross section of the Si interposer package model. Table 2 lists the material properties used in this simulation.

![Fig. 5 FEM model for warpage simulation. (a) Top view. (b) Cross section of LTCC package model. (c) Cross section of Si interposer package model.](image)

Table 2 Material properties used in simulation.

<table>
<thead>
<tr>
<th>Material</th>
<th>Elastic modulus [GPa]</th>
<th>Poisson's ratio</th>
<th>CTE [ppm/K]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>131</td>
<td>0.28</td>
<td>3.0</td>
</tr>
<tr>
<td>Fine line layer</td>
<td>20</td>
<td>0.3</td>
<td>17</td>
</tr>
<tr>
<td>LTCC</td>
<td>110</td>
<td>0.2</td>
<td>6</td>
</tr>
<tr>
<td>Organic sub.</td>
<td>25</td>
<td>0.16</td>
<td>16</td>
</tr>
<tr>
<td>UF @(\mu) bump</td>
<td>8.0/0.3</td>
<td>0.2</td>
<td>31/120</td>
</tr>
<tr>
<td>UF @C4 bump</td>
<td>7.0/0.25</td>
<td>0.2</td>
<td>32/110</td>
</tr>
</tbody>
</table>

Fig. 6 shows the simulation results. We simulated under the condition that it was unconstrained at 180°C, and analyzed the displacement at 25°C. The simulation results showed a dramatic drop in warpage when the LTCC were used. LTCC substrate can reduce the displacement to \(1/5\) of the Si interposer's displacement, which improves its reliability.

![Fig. 6 Simulation results of warpage. (a) LTCC package. (b) Si interposer package.](image)

V. ELECTRICAL PERFORMANCE ANALYSIS

The data transmission speed between the packages becomes higher and higher with the increase in the ICT systems bandwidth. A 28-Gb/s SerDes IC was developed [7], [8] and a 56-Gb/s standardization is currently being discussed [9]. Therefore, a lower loss is required for a package substrate. Since ceramics have a lower loss tangent, the LTCC substrate exhibits a good high-frequency property. Fig. 7 shows the measurement results of a line in the LTCC substrate. The structure is an 30 \(\mu\)m wide strip line, as shown in Fig. 8, and it is 15 mm long. Table 3 classifies the material characteristic. The channel loss of the LTCC substrate line is -1.7dB at 14GHz.
VI. CONCLUSION

We proposed an LTCC package with fine line layers. Due to the introduction of an LTCC substrate that decreases the shrinkage and void in the XY direction, fine line layer patterns with a line/space of 2/2 μm could be formed. Thereby, the LTCC package can now have an arrangement of 8 row escape routing lines between the pads with a 55 μm pitch. We showed that the routing between the ASIC and HBM can be designed using three layers of single-sided fine line layers on the LTCC substrate.

In addition, we have conducted both warpage and electrical performance analyses. The results from the warpage analysis using a FEM simulation showed that the LTCC substrate can reduce the displacement to 1/5 of the Si interposer's displacement, which helps improve the reliability. The results from the electrical performance analysis showed that the LTCC substrate has a low channel loss of -1.7dB at 14GHz.

We fabricated a prototype package and demonstrated the possibility of HBM.

REFERENCES


