Silicon-Package Co-Design of a 45nm 200MHz Bandwidth CMOS RF-to-Serdes Transceiver System on Chip (SoC)

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Abstract — In this paper we detail the silicon-package electrical co-design of a 45nm CMOS, 400MHz to 4GHz, 3GPP TDD & FDD, RF-to-Serdes base station transceiver system on chip (SoC). Electrical optimization of the silicon-package RF paths, to achieve desired performance, was achieved through a coupled circuit-to-electromagnetic co-design modeling and simulation flow. Laboratory measurements, on a real SoC system, are presented that validate the integrity of the modeling and simulation methodology.

Keywords — CMOS; RF-to-bits; Silicon-Package Co-Design; RF figure of merits (FOM)

I. INTRODUCTION

Increasing mobile data demands are pushing cellular network capacity. Massive MIMO base stations with large antenna arrays and smaller cell sizes demand higher integration in radio transceivers than what is available [1]. The advances in CMOS process and packaging technologies enable us to integrate a whole system on a single chip (SoC, system on chip) or on a package module (SoP, system on package) [2]. In these systems, analog/RF electronics and digital circuitries co-exist. Though these new technologies bring us new topologies for system integration, they also bring us new challenges in system design. To fully utilize the benefits of these new hardware technologies, concurrent physical and electrical design of silicon and package is critical in order to ensure highest performance, cost-effective solutions. The electromagnetic interaction between the silicon and the system (viz. package and PCB) of the RF-to-Serdes/Bits transmit and receive paths can impact the overall performance of the device [3-5]. In this paper we detail the electrical co-design modeling and analysis methodology that we developed to characterize a CMOS RF-to-Serdes/Bits transceiver SoC packaged in a 13x13mm² flip-chip BGA (ball grid array). In Section II we provide the high-level overview of the mixed-signal transceiver SoC circuit blocks. Section III covers the package and PCB physical designs. The iterative physical design tuning and electrical optimization co-design scheme is discussed in Section IV. Findings and observations are covered in Section V along with laboratory silicon measurements.

II. TRANSCEIVER SoC DESCRIPTION

A detail description of the CMOS RF-to-bits transceiver is provided in [6]. We summarize here the main building blocks and provide a high-level overview of the functionalities of each block. Fig. 1.0 below shows the schematic of the SoC. The SoC has 4x5Gbps serdes interface that supports all 3GPP (3rd Generation Partnership Project) bands from 400MHz to 4GHz with 200MHz instantaneous RF bandwidth (BW). It includes two transmitters (TX), two receivers (RX), and one high BW receiver (FBRX) for TX digital pre-distortion feedback (DPD), antenna tuning or network listening. Three integrated RF PLLs (phase-lock loop) provide independent LO (local oscillator) frequencies. Digital processing includes ADC decimation, DAC interpolation, filtering, and automatic RX gain control (AGC). Calibration, compensation, synchronization, and built-in-self-test with RF loop-back are integrated.

The SoC consumes 5Watt/6.5Watt in TDD/FDD (time domain duplexing/frequency domain duplexing) modes at maximum TX/RX/FBRX bandwidths of 200/100/200MHz and 40Gbps serdes I/O rate with +12dBm TX RF Pout (output power) when operating at 2.7GHz. Power consumption scales with TX power, RF BW, and serdes rates. The 7x7mm² SoC uses a 45nm low leakage CMOS process and contains an ARM M4F processor for control, calibration and compensation.
III. PACKAGE & PCB DESIGN DETAILS

The device is packaged in a 13x13mm² fcBGA (flip-chip ball grid array 0.8mm pitch multi-layer stack-up with standard BGA substrate materials). Fig. 2.0 below shows a 2-D view of the package and the major interfaces. The critical interfaces for this device are the RF transmit (TX) and receive (RX) paths, the analog serdes TX and RX, and the high-speed clock signals.

![Fig. 2. 2-D floorplan of package routing showing critical interfaces of SoC.](image)

The PCB EVM (evaluation module) developed for the design’s electrical characterization and validation is multilayered with approximate size of 153mm x 68mm. Fig. 3 below shows a 2-D view of the area of the PCB for the critical interfaces.

![Fig. 3. 2-D floorplan of PCB routing showing critical interfaces of SoC.](image)

The PCB dimension is approximately 153mm x 68mm and has 12 metal layers with standard FR-4 dielectric. Both the package and PCB physical designs were optimized by following good design practices to improve signal integrity (SI), power integrity (PI), and electromagnetic integrity (EMI).

IV. ELECTRICAL CO-DESIGN METHODOLOGY

Operating parameters, cost, and design considerations impact RF-to-Serdes transceiver performance and, subsequently, the RF and Serdes signal quality. Consequently, ensuring the SoC meets specification is essential in RF communications. Across various implementations of RF-to-Serdes transceivers there are standard electrical performance metrics/figure of merit (FOM) that are employed to characterize system design performance. In this paper we focus on a few critical system-level RF performance metrics – namely the transmit (TX) power, the adjacent channel leakage ratio (ACLR), the error vector magnitude (EVM) - an alternative to bit error ratio measurement, BER, the noise floor (NF), and then input power third order intercept point (IIP3) among others.

![Fig. 4. System-Level Co-Design Modeling & Analysis Flow.](image)

One main component of the system that impacts these FOMs is the integrity of the signal path/channel. Fig. 4.0 above shows the system physical and electrical co-design methodology that was adopted to characterize the quality of the channel. The input to the flow includes manufacturing and assembly guidelines for the package and PCB. The initial package and PCB physical RF and Serdes channels routing were optimized by adopting appropriate SI/PI/EMI design practices. Amongst the best practices were stack-ups optimizations, impedance control, crosstalk minimization, via/layer transition optimization, power/ground nets noise coupling isolation techniques, among others. Once physical designs optimizations were completed, a coupled circuit-electromagnetic system-level flow, discussed in detail in [6-8], was employed to perform the transient analysis. S-parameters for package and PCB were extracted using a frequency 3-D full wave solver and these models were combined with transistor level spice netlists for the system-level analysis in Cadence ADE (analog design environment). The optimization of the physical designs and system-level transient analyses were performed iteratively until desired performance was achieved.
V. FINDINGS & OBSERVATIONS

To validate the performance of the system predicted through co-design modeling and analysis methodology, as detailed in Section IV above, selective 3GPP standard RF conformance testing were performed [7]. These tests typically focus on the transmitter and receiver characteristics. We present here, the main TX and RX measurements results obtained on the SoC product (see Fig. 5–8). Table 1 summarizes the specification and the RF FOMs measurements that were achievable on the final product. Approximately 10-40% improvement, in electrical performance, was achievable from original to final package and PCB designs, through co-design approach. Adoption of the co-design methodology, early in the design flow, helps to optimize performance, cost, and improves time to market.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Measurements</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>45nm CMOS</td>
</tr>
<tr>
<td>Architecture</td>
<td>zero-IF RX &amp; TX</td>
</tr>
<tr>
<td>Frequency Coverage</td>
<td>400-4000</td>
</tr>
<tr>
<td>Modulation</td>
<td>60MHz (3x LTE20)</td>
</tr>
<tr>
<td>Frequency</td>
<td>2.6</td>
</tr>
<tr>
<td>Power</td>
<td>0 (composite)</td>
</tr>
<tr>
<td>ACLR</td>
<td>-57</td>
</tr>
<tr>
<td>EVM</td>
<td>0.5 (1x LTE20)</td>
</tr>
<tr>
<td>Noise</td>
<td>-159</td>
</tr>
<tr>
<td>Power</td>
<td>0.5 (a)</td>
</tr>
</tbody>
</table>

Note:
(a) TX only, without DAC, (b) External LNA: 18dB gain, 1.1dB NF, (c) RX only, without ADC, (d) LNA power 35mW de-embedded

Table 1. Specification and measured RF FOMs.

CONCLUSIONS

In this paper we demonstrate the successful development and application of a co-design modeling methodology for the design of a 200MHz bandwidth CMOS RF-to-Serdes SOC.

REFERENCES